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(54) Data transmission system and apparatus providing multi-level differential signal transmission.

(57) A data transmission system which provides differential transmission of a binary interface formed by a plurality of binary input signals. The binary interface is encoded by an encoder into a corresponding multi-level differential interface formed by a plurality of multi-level signals, such correspondence being in accordance with a pre-selected code conversion table, and the respective multi-level signals are transmitted over respective transmission channels. Upon reception at a decoder, the signs of the differences between respective pairs of the multi-level signals are detected, and in accordance with such signs binary values are assigned to respective binary output signals of the decoder in accordance with the inverse of the code conversion table employed for encoding. Differential transmission achieves immunity from common mode noise, and multi-level encoding permits differential transmission over fewer channels than would be required for binary differential transmission.

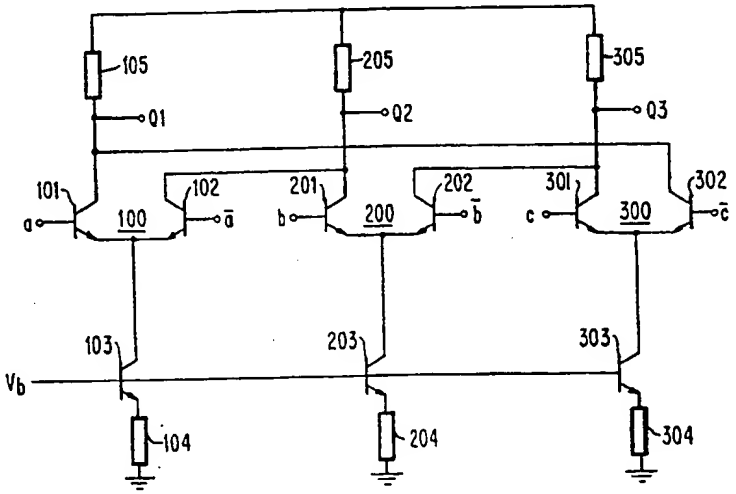

FIG.3

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FIELD OF THE INVENTION

The invention relates to a data transmission system wherein binary data is transmitted in the form of multi-level differential signals over respective transmission channels, and the received signals are decoded on the basis of the signs of the differences between pairs of such signals rather than their magnitudes. A high transmission rate and immunity from common mode noise is thereby achieved, and with fewer channels than would be required for differential transmission in binary form. As used herein the term "multi-level" refers to more than two possible levels, two levels being characteristic of binary signals.

Transmission of binary data is most commonly effected by employing a binary single-ended interface, the signals in the respective transmission channels corresponding to respective bits of the binary data. The group of signals on all channels is referred to as an "interface", and in the absence of noise a binary single-ended interface makes the most efficient use of channel capacity. Such interfaces are subject to transmission error when there is common mode noise on the channels; i.e., noise occurring substantially to the same extent on all channels, since decoding of the received signals requires detection of their amplitudes relative to a fixed reference level.

Multi-level rather than binary interfaces have been employed in order to obtain an increased information transmission rate over a given number of channels, the value of the signal in each channel being at any of several possible levels which respectively correspond to several binary data bits. See, for example, U.S. Patent No. 4,606,046. However, such interfaces still encounter the common mode noise problem, since decoding of the received multi-levels requires comparison with a fixed reference level.

The problem of common mode noise in transmission can be substantially eliminated by encoding the binary data in differential form, each bit thereof being represented by the difference between signals on a pair of lines, since such a difference will not be affected by equal changes in the amplitudes of the signals on both lines. Also, only the sign (rather than the magnitude) of the signal difference need be detected. However, binary differential transmission necessitates two lines per bit, which increases costs. Sometimes, there are not even enough IC package pins available.

Consequently, there is need for a transmission system which provides a high information transmission rate together with common mode noise suppression, and which requires fewer transmission channels than necessary for binary differential transmission.

SUMMARY OF THE INVENTION

A data transmission system in accordance with the invention provides multi-level differential transmission of binary data over a plurality m>2 of transmission channels such as wires, lines, frequency bands, etc. The system comprises an encoder for receiving the binary input signals to be transmitted and encoding such binary interface into a multi-level differential interface, each multi-level signal being assigned a value at any of a number (n) of different levels and all such signals having different values. For optimum utilization of channel capacity, (n) should be equal to (m). The value so assigned to each multi-level signal is derived as an arithmetic combination of the binary values of a respective group of the binary signals, i.e. two or more, such correspondence being in accordance with a pre-selected code conversion or so-called "mapping" table. The encoder supplies the respective multi-level signals to the respective transmission channels. A decoder receives the transmitted multi-level signals, determines the signs of the differences in values of respective pairs thereof, and in accordance with such sign differences assigns binary values to respective binary output signals, such assignments being in accordance with the inverse of the same code conversion table as employed for encoding. This procedure recovers the original transmitted binary interface. Immunity from common mode noise is obtained as a result of differential signal transmission, and the number of channels which are required is less than would be necessary for differential transmission of the original binary interface.

The invention also relates to an encoder and a decoder for use in such a system.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows in block form a data transmission system in accordance with the invention;

Fig. 2 is an example of a code conversion table for converting a binary input signal into a multi-level signal;

Fig. 3 is a circuit drawing of an encoder such as may be employed in the system of Fig. 1. and Fig. 3a shows a code conversion table for encoding and decoding;

Fig. 4 is a circuit drawing of a decoder such as can be employed in the system in Fig. 1;

Fig. 5 is a comparison of significant characteristics of single-ended and differential transmission of binary signals and multi-level signals.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Binary data symbols can be transmitted in the form of signals of different values over respective transmission channels such as, for example, the wires of a transmission bus; each permutation of signal values representing a particular data symbol. The simplest encoding of data into signals is binary, the value of each signal being at either a high (V_h) or a low (V_o) voltage level. Thus, two wires can carry two bits of binary information, one bit per wire. A ground reference wire is also necessary. Binary differential encoding obviates the need for a ground wire, but at least two wires have generally been considered necessary for each bit since the value of each bit is then represented by the sign (+ or -) of the difference between the signals on a pair of wires. Thus, for encoding two bits it is necessary to employ four wires, the values of the bits being determined from the signs of the differences between the signals on two different pairs of such wires, such as (w_1-w_2) and (w_3-w_4). Since there are six possible pairs of the four wires, at least one more bit could be transmitted by assigning to such bit the sign value of another pair, such as (w_1-w_3), which can be chosen independently of the sign values of the first two pairs. In general, if the number of wires is (m) the number (p) of different wire pairs will be $\frac{1}{2}m(m-1)$. To make use of this, however, it is necessary for the signal on each wire to have more than just two possible levels. By employing additional signal levels rather than additional wires, it is possible to differentially encode a greater number of bits than the number of wires.

In general, a multi-level differential encoder may have (m) wires over which information is differentially transmitted using (n) different levels. That is, the value of the signal on each wire can be at any of the levels 1, 2, ...n. In order to determine the values of the signals on each of the (m) wires from the differences between pairs of such signals (differential detection) two conditions should be met:

(1) no two signals should be at the same level; and

(2) each of the n levels should be assigned to at least one wire signal.

If m>n, one or more signal levels will have to be assigned to at least two wires. The difference between the values of the signals on that pair of wires does not convey any information, and so the information transmission rate of the wires is not fully utilized. If m<n, then for each transmission there will be some signal levels which cannot be assigned to wires and so cannot be used to convey any information. The optimum condition is achieved when m = n, i.e.,the number of channels should be equal to the number of signal levels.

Since each permutation of the values of the signals on all wires constitutes a "symbol", the number of symbols which can be transmitted is n! That is, the signal on the first wire can have any of n values, the signal on the second wire can have any of (n-1) values, and so on to the last wire. The four-wire encoder discussed above would therefore be capable of transmitting 4! = 24 different symbols, which exceeds 4 bits of information (2^4 = 16).

The encoding operation for assigning signal values at any of n levels to n channels may be carried out by the following algorithm:

(1) assign any value to the signal on wire w_1;

(2) for any wire w_i from w_2 to w_{n-1}, assign a value which differs from those assigned to wires w_1 to w_{i-1};

(3) assign the remaining value to the signal on wire w_n.

For example, for a three-wire, three-level encoder, the three levels being $V_1<V_2<V_3$, assign any of such levels, e.g. V_3, to the signal on wire w_1. For the signal on wire w_2 the assigned level must be V_1 or V_2, e.g. V_1. This leaves only V_2 as the level t be assigned to the signal on wire w_3. By encoding in this way, it is seen that all wires will be at different signal levels. After transmission the values of the signals on the respective wires can be determined by detecting only the signs of the differences between the signals on each pair of wires. In the present example, sorting the differences between the values of the signals on pairs of the wires given the following results:

wire pairs	signal difference	wire sequence
(w_1-w_2)	$V_3-V_1>0$	$w_1>w_2$
(w_2-w_3)	$V_1-V_2<0$	$w_2>w_3$
(w_1-w_3)	$V_3-V_2>0$	$w_1>w_3$

Consequently, $w_1>w_3>w_2$, and so the signal sequence must be V_3 on wire w_1, V_2 on wire w_3, and V_1 on wire w_2. In the wire order w_1, w_2, w_3, such signal sequence is V_3, V_1, V_2, which is the same as the signal levels originally assigned to those wires. This correspondence will, of course, be true regardless of which of the levels (V_1, V_2 and V_3) were originally assigned to the signals on the respective wires.

The decoding operation can be effected using the following algorithm;

(1) detect the signs S_{ij} of the differences (v_i-v_j) between the values of the signals on any pair of wires in positions i and j in the wire sequence;

(2) find the signal value v_i for which $S_{ij}=1$ for all j, and assign that signal value to wire w_i;

(3) disregard signal value v_i and sign S_{ij};

(4) repeat steps (2) and (3) until all signal values have been assigned.

The signal values assigned by this iterative procedure are determined by their sequential order, each being one level below that of the preceding assigned signal value. The last signal value assigned will be at the lowest or "zero" level.

Referring to Fig. 1, there is shown in block form a data transmission system in accordance with the invention. Although any number of lines and signal levels can be employed, to simplify the description Fig. 1 shows a 3-line 3-level system. It comprises an encoder 1 having three inputs for receiving in parallel three binary input signals, and three outputs each of which is assigned a value at any of three voltage levels $V_1<V_2<V_3$, the outputs being respectively connected to respective channels w_1, w_2, w_3 are respectively connected to three inputs of a decoder 2 having three outputs at which three binary output signals are produced.

The encoder assigns signal values to the respective lines in accordance with an arithmetic combination of the values of respective groups of the binary input signals, such assignments being pursuant to any arbitrarily selected code conversion table such that no two line signals will have the same value; for example, the code conversion table shown in Fig. 2. This was formulated by assigning a different one of the six possible multi-level differential interfaces to each of six possible combinations of the binary input signals. It will be noted that since $3! = 6$, while $2^3 = 8$, with three lines there will be two possible binary input interfaces which cannot be represented and so cannot be transmitted by three-wire differential transmission.

In general, with (n) levels the number of different multi-level interfaces is n!, while the number of interfaces which can be formed by (p) signals is 2^p. When $n=m$, the number of channels, the value of p will be $\frac{1}{2}n(n-1)$. Since n! and 2^p will almost always be different, it therefore is not possible to map all possible binary interfaces with respective multi-level interfaces. For example, if $n=m=4$, then $p=6$ and so there will be 6 binary signals which can form $2^6=64$ different binary interfaces of which only $4!=24$ can be matched to different multi-level interfaces at the output of the encoder. It is possible to utilize only 4 binary input signals, providing 16 different binary interfaces, and employ the remaining 8 possible combinations of the decoder outputs for transmission of handshaking, synchronization, error and other information.

Upon reception of the three multi-level signals at the decoder, the signs of the differences between different pairs of such signals, (w_1-w_2), (w_2-w_3) and (w_1-w_3),are detected. As described above, from the signs of such differences the values of the signals on each of the three input lines are determined. The three outputs are then assigned binary values corresponding to the input signals in accordance with the same code conversion table as had been employed for encoding, as shown in Fig. 2. For example, if the three differences between the line signals establish that $w_1<w_2$, $w_2>w_3$, and $w_1>w_3$, it follows that $w_2>w_1>w_3$. Consequently, line w_1 has the signal value V_2, line w_2 has the signal value V_3 and line w_3 has the signal value V_1. This sequence, V_2, V_3, V_1, is seen from the code conversion table in Fig. 2 as corresponding to binary code 011. Consequently, decoder 2 assigns that sequence of values to the binary output signals.

The encoder and decoder can be implemented in any of various types of integrated circuit technologies, including but not limited to CMOS, BiCMOS and Bipolar. For purposes of illustration, they have been shown in Figs. 3 and 4 as bipolar transistor circuits but it is clear that field-effect circuits could alternatively be used.

The 3-level 3-line encoder in Fig. 3 receives binary input signals a, b, c of descending order of significance at the inputs of three successive differential amplifier stages 100, 200 and 300. Each such stage consists of a pair of emitter-coupled transistors coupled to a constant current source in the form of a transistor biased to operate on the horizontal part of its collector-current characteristic. Thus, stage 100 comprises transistors 101 and 102, the emitters of which are connected to the collector of a transistor 103, the emitter of transistor 103 being returned to ground by a resistor 104. The base of transistor 103 is connected to a source of bias voltage B_b, which biases it so that its collector current remains substantially constant. The collector of transistor 101 is connected by a resistor 105 to a supply source V_d. The elements of differential amplifier stages 200 and 300 are the same as those of 100, corresponding elements thereof being identified by corresponding numerals in the 100, 200 and 300 series. The collector of transistor 102 in stage 100 is cross-connected to the collector of transistor 201 in stage 200, the collector of transistor 202 in stage 200 is cross-connected to the collector of transistor 301 in stage 300, and the collector of transistor 302 in stage 300 is cross-connected to the collector of transistor 101 in stage 100. The bases of transistors 101, 201 and 301 respectively receive the binary input signals a, b, c, and the bases of transistors 102, 202, and 302 respectively receive the complements of such signals $\bar{a}$, $\bar{b}$ and $\bar{c}$. This presumes that each input binary signal and its complement is available. If only single-ended binary signals are available, the bases of transistors 102, 202 and 302 can be connected instead to a source of reference voltage at a level between the levels corresponding to a "1" and a "0" value of a binary signal. The collector voltage of transistor 101 is taken as the output signal Q1 of stage 100, the collector voltage of transistor 201 taken as the output signal Q2 of stage 200, and the collector voltage of transistor 301 is taken as the output signal Q3 of stage 300. Q1, Q2 and Q3 together constitute a tri-level code combination which corresponds, or is "mapped", to the input binary signal in accordance with the code conversion table in Fig. 3a, the signal levels 0, 1, 2 in such table corresponding to low (V_1), intermediate (V_2) and high (V_3) different voltage levels produced at the outputs of the encoder circuit and which preferably are equally spaced.

The signal Q1 is determined by the sum of the currents through transistors 101 and 302 and so corresponds to the sum of the signals "a" and "$\bar{c}$" at the bases of those transistors. If both those signals are a binary "0", transistors 101 and 302 will both be in a low or non-conductive state. There will then be minimal current in resistor 105 and so the value of signal Q1 will be at the high voltage level V_3. If the "a" and the "$\bar{c}$" signals are both binary "1"s, transistors 101 and 302 will both be fully conductive. Since only one of the transistors in each differential stage at a time can be fully conductive, and the total emitter current of both remains constant, if such current is denoted as one current unit there will therefore be a total of two current units through resistor 105. The value of signal Q1 will then be at the low voltage level V_1. Finally, if the "a" and "$\bar{c}$" signals are a combination of a "0" and "1", one of transistors 101 and 302 will be in the low conductive state and the other will be fully conductive. There will then be one current unit through resistor 105, and so the value of signal Q1 will be at the intermediate voltage level V_2.

Since a "1" input bit produces one current unit at the collector of the transistor which receives it, resulting in a one level reduction from the maximum level V_3 of the output signal at such collector, the value of the signal Q1 will be proportional to the difference between V_3 and the arithmetic sum of "a" and "$\bar{c}$". If the value of signal Q1 is denoted V_{Q1}, this can be expressed as:

$$V_{Q1} = V_3 - \Delta V(a + \bar{c}),$$

where ΔV is the voltage difference between successive signal levels. If the signal levels V_1, V_2, V_3 signify 1, 2 and 3, and levels 1 and 2 are the same as those for the binary values "0" and "1", this equation becomes

$$V_{Q1} = 2-(a + \bar{c}),$$

A similar analysis applies to the output signals Q2 and Q3 which respectively correspond to $(\bar{a} + b)$ and $(\bar{b} + c)$, resulting in

$$V_{Q2} = 2-(\bar{a} + b),$$
$$V_{Q2} = 2-(\bar{b} + c).$$

Applying these relationships to, for example, the first line of the table in Fig. 3a, the input binary signal is 001 and so $a=0$, $b=0$, $c=1$, and also $\bar{a}=1$, $\bar{b}=1$, and $\bar{c}=0$. Substituting these values in the above equations, it results that $V_{Q1}=2$, $V_{Q2}=1$, $V_{Q3}=0$. For the second line in the table, the input binary signal is 010 and so $a=0$, $b=1$, and $c=0$. Substituting these values in the above-equations, it results that $V_{Q1}=1$,

$V_{Q2} = 0$, $V_{Q3} = 2$. The outputs corresponding to the binary signals in the remaining lines of the table are similarly derived.

It should be noted that although the 3-line 3-level encoder in Fig. 3 derives its outputs in accordance with the arithmetic sums of pairs of the binary input signals, when a greater number of interface levels is employed the outputs of the encoder will depend on combinations of groups of more than two of the input signals. For example, with a 4-level interface each multi-level output signal will be derived from an arithmetic combination of a group of 3 of the binary input signals.

It should also be noted that the division of current between the transistors of any of the differential stages depends only on the relative base voltages of the two transistors of such state, not on the absolute values of such voltages. Consequently, if both increase or decrease by the same amount that will not alter the current in the collector resistor of such stage. Thus, common mode noise affecting both base voltages will have no effect on the output of such stage.

Fig. 4 shows a bipolar implementation of a decoder for the multi-level signals Q1, Q2, Q3 respectively received over the three respective lines of a transmission bus from an encoder such as that in Fig. 3. Similar to the encoder, the decoder also comprises three differential amplifier stages 400, 500 and 600, one of each possible pair of signals, each including a pair of emitter-coupled transistors connected to a constant current source in the form of a transistor biased to operate on the horizontal part of its collector-current characteristic. Stage 400 includes transistors 401 and 402, the emitters of which are connected to the collector of a transistor 403 which serves as a constant current source, the emitter of transistor 403 being returned to ground by resistor 404. The base of transistor 403 is connected to a source of bias voltage V_b to maintain a substantially constant collector current. The collectors of transistors 401 and 402 are respectively connected by resistors 405 and 406 to a source of supply voltage V_d. The elements of differential stages 500 and 600 are the same as those of 400, corresponding elements thereof being identified by corresponding numerals in the 400, 500 and 600 series.

The respective binary outputs b_1 b_2, b_3 produced by the decoder are obtained at the collectors of transistors 401, 501 and 601. Considering transistor 401, its collector current is determined by the difference (Q1-Q2) between the line signals Q1 and Q2 respectively supplied to the bases of transistors 401 and 402. Since the total current through both transistors is held constant, and can be designated as one current unit, there cannot be more than one current unit through either collector resistor 405 or collector resistor 406. Consequently, there will be one current unit through resistor 405 when the line signal Q1 at the base of transistor 401 exceeds the line signal Q2 at the base of transistor 402. There will be substantially no current through collector resistor 405 when Q1<Q2. The collector voltage of transistor 401, which constitutes the binary output signal b_1, therefore changes from the maximum or '1" level to the minimum or "0" level when the difference (Q1-Q2) changes from negative to positive. Consequently,

$$b_1 = \text{Sign}(Q2-Q1).$$

By a similar analysis, the binary output signal b_2 at the collector of transistor 501 in stage 500, and the binary output signal b_3 at the collector of transistor 601 in stage 600, are given by

$$b_2 = \text{Sign}(Q3-Q2), \text{ and}$$
$$b_3 = \text{Sign}(Q1-Q3).$$

The table in Fig. 3a shows how these relationships result in differential decoding of the input tri-level signals Q1, Q2, Q3 to derive output binary signals b_1, b_2 b_3. For example, the first line of such table is for an input signal such that Q1 = 2, Q2 = 1 and Q3 = 0. The sign of (Q2-Q1) is therefore negative, resulting in binary signal $b_1 = 0$; the sign of (Q3-Q2) is also negative, resulting in binary signal $b_2 = 0$; and the sign of (Q1-Q3) is positive, resulting in binary signal $b_3 = 1$. The decoder output signals b_1, b_2, b_3 therefore is again 001.

The second line of the table in Fig. 3a is for an input interface such that Q1 = 2, Q1 = 1, Q3 = 0. Consequently, (Q2-Q1) is negative and so $b_1 = 0$; (Q3-Q2) is positive and so $b_2 = 1$; and (Q1-Q3) is negative and so $b_3 = 0$. The decoder outputs b_1, b_2, b_3 therefore correspond to 010. In this way the original signals are recovered.

Although the number of different symbols can be transmitted over an n-channel n-level differential interface is equal to n!, the rate at which information can be transmitted does not increase as fast as this would imply as the value of "n" is increased. That is because, due to the time constant of each channel,

with an increasing number of signal levels a longer time is required for all signals to finally reach or "settle" at their assigned levels. If the amount of information that can be transmitted per unit time is denoted as the Information Transmission Rate ("ITR"), and the number of symbols that can be transmitted per unit time is denoted as the Symbol Transmission Rate ("STR"), the ITR is given by

$$ITR = STR \log_2 T$$

where $\log_2 T$ is the number of bits which can be represented during each transmission.

The table in Fig. 5 shows a comparison between single-ended and differential transmission for different values of "n", the number of signal levels. It is seen that in the case of single-ended transmission the information transmission rate for a multi-level interface is lower than for a binary differential interface, while the reverse is true for differential transmission. This is due to the higher redundancy inherent in binary differential interfaces.

While the invention has been described with reference to certain preferred embodiments thereof, it will be apparent to those skilled in the art that various modifications and adaptations thereof may be made without departing from the essential teachings and scope of the present invention as set forth in the ensuing Claims.

FIGURE REFERENCES:

Fig. 1 left hand: 3-bit binary signal; middle: transmission channels; right hand: 3-bit binary signal.
Fig. 2 left column: value; middle column: binary code; right column: multi level code;
Fig. 5: left columns: single-ended transmission; right columns: differential transmission; first row: signal levels; second row: channel; third row: No. of symbols; fourth row: bits per symbol; fifth row: settle time.

Claims

1. A multi-level differential encoder for use in a data transmission system wherein a binary interface formed by a plurality (p)of binary input signals is transmitted over a plurality m>2 of transmission channels, p being equal to or less than $\frac{1}{2}m(m-1)$; said encoder comprising:
   means for receiving the binary input signals and deriving therefrom a multi-level interface formed by said, number (m) of multi-level signals, the respective multi-level signals being assigned values at respectively different ones of said number (m) of different levels;
   the value so assigned to any multi-level signal corresponding to an arithmetic combination of the binary values of a respective group of the binary input signals, such correspondence being in accordance with a pre-selected code conversion table; and
   means for supplying the respective multi-level signals to the respective transmission channels.

2. An encoder as claimed in Claim 1, wherein the different levels of the multi-level signals are equally spaced from each other.

3. An encoder as claimed in Claim 2, wherein the values assigned to the respective multi-level signals respectively correspond to the arithmetic sum of the binary values of respective groups of said binary input signals.

4. An encoder as claimed in Claim 1 wherein said encoder comprises a succession of differential amplifier stages, the respective stages receiving the respective binary input signals and deriving therefrom the respective multi-level signals in accordance with said pre-selected code conversion table.

5. An encoder as claimed in Claim 4 wherein the differential amplifier stages each comprise a pair of transistors coupled to a substantially constant current source, so that the total current conducted by both transistors of each such pair remains substantially constant.

6. A multi-level differential decoder for use in a data transmission wherein a binary interface formed by a plurality (p) of binary input signals is transmitted in the form of a plurality m>2 of differential signals over said number (m) of transmission channels as multi-level signals having values at respective ones of said number (m) of different levels, p being equal to or less than $\frac{1}{2}m(m-1)$; said decoder comprising: means for receiving the multi-level signals and deriving therefrom a binary interface

formed by said number (p) of binary output signals, said binary output signals being assigned binary values corresponding to the signs of the differences between the values of respective pairs of said multi-level signals;

the correspondence between said binary values of the binary output signals and said sign differences being in accordance with a pre-selected code conversion table such that the binary interface formed by the (p) binary output signals is the same as the binary interface formed by said binary input signals.

7. A decoder as claimed in Claim 6 wherein said decoder comprises a succession of differential amplifier stages, the respective stages receiving said respective pairs of multi-level signals and deriving therefrom the respective binary output signals in accordance with said pre-selected code conversion table.

8. A decoder as claimed in Claim 7 wherein the differential amplifier stages each comprise a pair of transistors coupled to a substantially constant current source, so that the total current conducted by both transistors of each such pair remains substantially constant.

9. A data transmission system for differential transmission of a plurality m>2 signals of transmission channels of a binary interface formed by a plurality (p) of binary inputs, p being equal to or less than $\frac{1}{2}m(m-1)$; said encoder comprising: an encoder for encoding the binary input signals into said number (m) of multi-level signals so as to form a multi-level interface, the respective multi-level signals being assigned values at different ones of said number (m) of different levels; the value so assigned to any multi-level signal corresponding to an arithmetic combination of the binary values of a respective group of the binary input signals, such correspondence being in accordance with a pre-selected code conversion table; said encoder supplying the respective multi-level signals to the respective transmission channels; and

a decoder for receiving from said transmission channels the multi-level interface formed by the (m) transmitted multi-level signals and deriving therefrom a corresponding binary interface comprising a plurality (p) of binary output signals; said decoder being adapted to determine the signs of the differences in values of respective pairs of the multi-level signals and to assign binary values to the respective binary output signals corresponding to such sign differences, such correspondence being in accordance with the inverse of said pre-selected code conversion table;

the binary interface formed by the (p) binary output signals produced by said decoder being the same as the binary interface formed by the (p) binary input signals to said encoder.

10. A method of effecting differential transmission over a plurality of m>2 of transmission channels, w_1, w_2, ..., w_m, of a binary interface formed by a plurality (p) of binary input signals, p being equal to or less than $\frac{1}{2}m(m-1)$; such method comprising encoding the input binary interface to form a corresponding multi-level differential interface having (m) multi-level signals, and transmitting the respective multi-level signals over the respective channels; said encoding comprising the steps of:

(1) assigning to the multi-level signal transmitted over channel w_1 a value which is at any of a plurality (m) of different levels;

(2) for any channel w_i from w_2 to w_{m-1}, assigning to the multi-level signal transmitted over such channel a value which is at one of said (m) levels and which differs from the values assigned to the multi-level signals transmitted over channels w_1 to w_{i-1}; and

(3) assigning to the multi-level signal transmitted over channel w_m a value which is at the signal level remaining after values have been assigned to the multi-level signals on channels w_1 to w_{m-1}.

11. A method as claimed in Claim 7, wherein the values assigned to the respective multi-level signals respectively correspond to the arithmetic sum of the binary values of a respective group of said transmitted binary signals, such correspondence being in accordance with a pre-selected code conversion table.

12. A method as claimed in Claim 10, for decoding the multi-level interface formed by the (m) multi-level signals to derive (p) binary signals which form a binary interface the same as the transmitted binary interface the same as the binary interface, said decoding comprising the steps of:

(1) detecting the signs of the differences in the values of respective pairs of said multi-level

signals; and
(2) assigning binary values in accordance with the signs so detected to each of the (p) binary output signals, the relationship between said signs and said assigned binary values being in accordance with the inverse of said code conversion table.

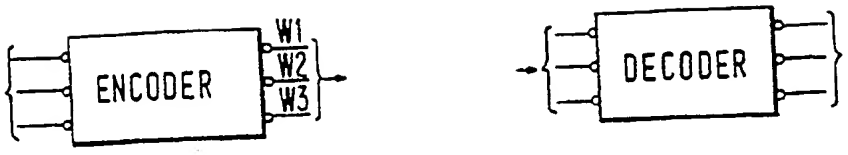

FIG. 1

		W1	W2	W3
0	000	V_1	V_2	V_3
1	001	V_1	V_3	V_2
2	010	V_2	V_1	V_3
3	011	V_2	V_3	V_1
4	100	V_3	V_1	V_2
5	101	V_3	V_2	V_1

FIG. 2

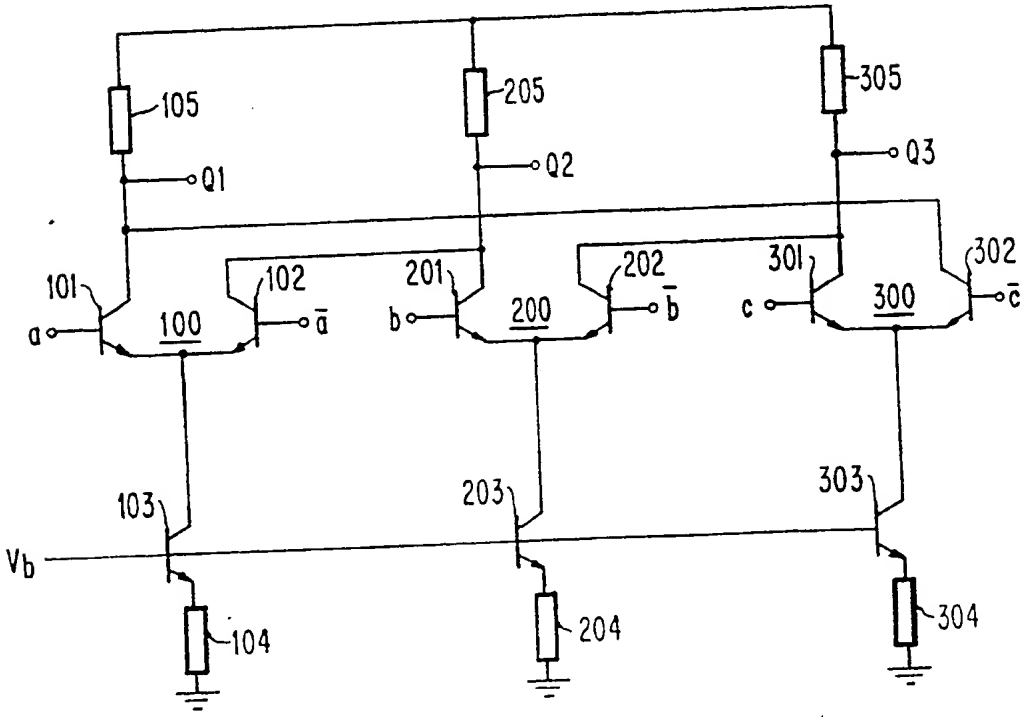

FIG. 3

a	b	c	Q1	Q2	Q3	b1	b2	b3
0	0	1	2	1	0	0	0	1
0	1	0	1	0	2	0	1	0
0	1	1	2	0	1	0	1	1
1	0	0	0	2	1	1	0	0
1	0	1	1	2	0	1	0	1
1	1	0	0	1	2	1	1	0

FIG.3a

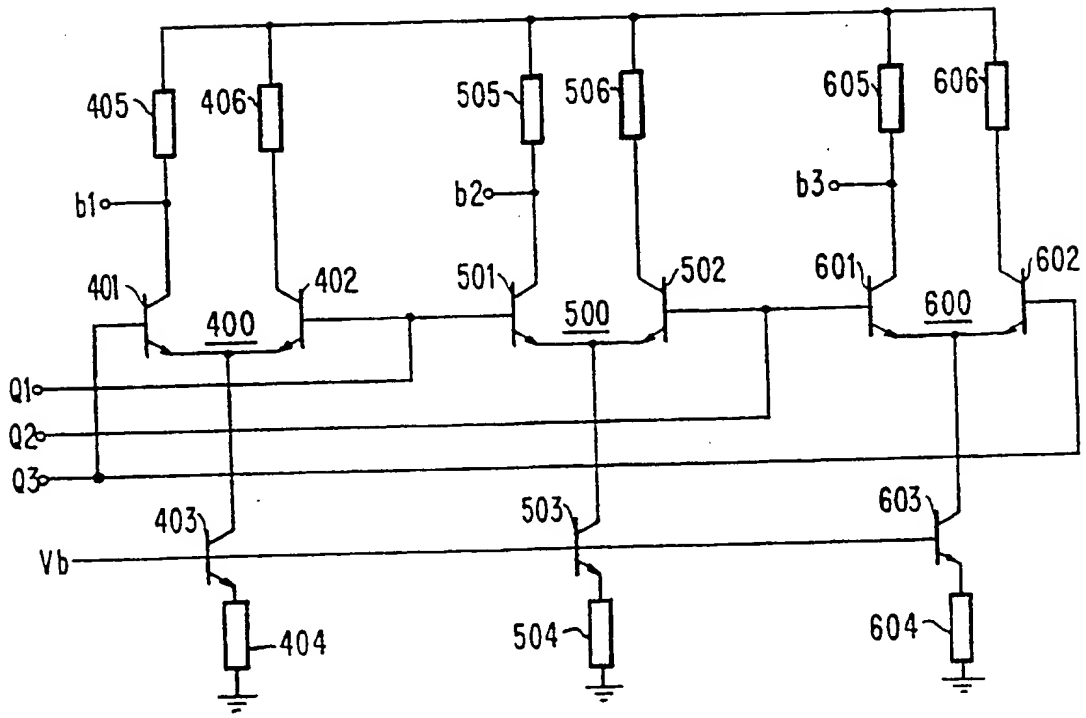

FIG.4

	2	n	2	n
	n	n	n	n
	2^{n-1}	n^{n-1}	$2^{n/2}$	n!
	n-1	$\log_2(n^{n-1})$	n/2	$\log_2(n!)$
	$\tau \ln(2)$	$\tau \ln(2n-2)$	$\tau \ln(2)$	$\tau \ln(n)$
ITR:	$\frac{n-1}{\tau \ln(2)}$	$\frac{\log_2(n^{n-1})}{\tau \ln(2n-2)}$	$\frac{n}{2\tau \ln(2)}$	$\frac{\log_2(n!)}{\tau \ln(n)}$

FIG. 5

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(54) Data transmission system and apparatus providing multi-level differential signal transmission.

(57) A data transmission system which provides differential transmission of a binary interface formed by a plurality of binary input signals. The binary interface is encoded by an encoder into a corresponding multi-level differential interface formed by a plurality of multi-level signals, such correspondence being in accordance with a pre-selected code conversion table, and the respective multi-level signals are transmitted over respective transmission channels. Upon reception at a decoder, the signs of the differences between respective pairs of the multi-level signals are detected, and in accordance with such signs binary values are assigned to respective binary output signals of the decoder in accordance with the inverse of the code conversion table employed for encoding. Differential transmission achieves immunity from common mode noise, and multi-level encoding permits differential transmission over fewer channels than would be required for binary differential transmission.

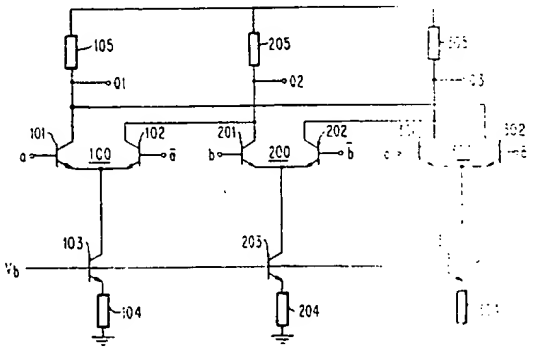

FIG.3

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EUROPEAN SEARCH REPORT

Application Number

EP 91 20 1138

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PROCEEDINGS OF THE INSTITUTION OF ELECTRICAL ENGINEERS vol. 126, no. 9, September 1979, STEVENAGE GB pages 893 - 900 TUCKER 'A technical history of phantom circuits' * figure 1 *	1,9,10	H04L25/49
A,D	WO-A-8 502 960 (AT&T) * abstract; figures 1,5 *	5,7,8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 DECEMBER 1992	SCRIVEN P.

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